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Charles A Johnson
Unisys Corporation
Law Department M.S. 4773
2470 Highcrest Road
Roseville, MN 55113

EXAMINER
VITAL, PIERRE M

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,488	ENGLIN ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed March 24, 2003 in response to PTO Office Action mailed December 18, 2002. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-20 have been presented for examination in this application. In response to the last Office Action, no claims have been amended. No claims have been canceled or added. As a result, claims 1-20 are now pending in this application.

3. The objection to the specification has been withdrawn due to the amendment filed March 24, 2003.

4. The rejection of claims 1-20 as in the Office action mailed December 18, 2002 (Paper No. 3) is respectfully maintained and reiterated below for Applicant's convenience.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 6, 7, 11 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Gallagher et al. (US 5,276,848).

As per claims 1, 6 and 16, Gallagher discloses a data processing system having a processor responsively coupled to a store-in cache memory which is responsively

coupled to a lower level memory {*i.e., processor 20, 22; cache 26a, memory 10b*} [Fig.2; col. 3, lines 25-58], the improvement comprising a flush buffer responsively coupled to said store-in cache memory and said lower level memory {*i.e., store buffer in SCL 12 positioned between L1 and L3*} [Fig. 1; col. 2, line 66 – col. 3, line 5].

As per claim 7, Gallagher discloses a flush buffer comprises a first flush buffer store and a second flush buffer store {*i.e., buffers up to 8 stores*} [col. 3, lines 4-6].

As per claim 11, Gallagher discloses the claimed invention as detailed above per claims 1 and 6. Gallagher further discloses selecting a particular location to a flush buffer {*i.e., obsolete data*} [col. 3, lines 1-3]; transferring data from said particular location to a flush buffer {*i.e., data stored in buffer for transfer*} [col. 3, lines 1-6].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-5, 8-10, 12-15, 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al (US5,276,848) and Jeddeloh (US6,460,114).

As per claims 2 and 12, Gallagher discloses the claimed invention as detailed above in the previous paragraphs. However, Gallagher does not specifically teach a tag

memory indicating whether a particular memory location has been modified as recited in the claim.

Jeddeloh discloses a tag memory indicating whether a particular memory location has been modified [col. 3, lines 44-49].

As per claims 3 and 17, Gallagher discloses the claimed invention as detailed above in the previous paragraphs. However, Gallagher does not specifically teach loading said flush buffer with data from said particular location within said store-in cache memory in response to said indication that said particular location has been modified as recited in the claim.

Jeddeloh discloses loading said flush buffer with data from said particular location within said store-in cache memory in response to an indication that said particular location has been modified [col. 3, lines 35-49].

It would have been obvious to one of ordinary skill in the art, having the teachings of Gallagher and Jeddeloh before him at the time the invention was made, to modify the system of Gallagher to include a tag memory indicating whether a particular memory location has been modified and loading said flush buffer with data from said particular location within said store-in cache memory in response to said indication that said particular location has been modified because it would have provided better memory access transactions control as taught by Jeddeloh by reducing the read latency associated with the search for target data [col.1, lines 59-60, col. 2, line 40] as taught by Jeddeloh.

As per claims 4 and 18, Gallagher discloses a flush buffer comprises a first flush buffer store and a second flush buffer store {*i.e., buffers up to 8 stores*} [col. 3, lines 4-6].

As per claims 5 and 19, Jeddeloh discloses the concept of a temporary register coupled to a store-in cache memory, a first flush buffer store and a second flush buffer store which routes said data from said particular location to an available one of said first flush store and said second buffer store {*i.e., posted write buffer capable of holding 8 cache lines (i.e., stores) used as temporary staging area*} [col. 3, lines 35-64].

8. As per claim 8, Gallagher discloses the claimed invention as detailed above per claims 6 and 7. However, Gallagher does not specifically teach a temporary register responsively coupled to a store-in cache memory, a first flush buffer store and a second flush buffer store as recited in the claim.

Jeddeloh discloses the concept of a temporary register coupled to a store-in cache memory, a first flush buffer store and a second flush buffer store {*i.e., posted write buffer used as temporary staging area*} [col. 3, lines 35-64].

As per claim 9, Gallagher does not specifically teach a tag memory indicating whether a particular memory location has been modified as recited in the claim.

Jeddeloh discloses a tag memory indicating whether a particular memory location has been modified [col. 3, lines 44-49].

9. As per claim 10, Gallagher discloses the claimed invention as detailed above per claim 6. However, Gallagher does not specifically teach a logic circuit responsively coupled to said tag memory, said store-in cache memory and said temporary register which routes data from a particular location from said store-in cache memory to said temporary register when said indication is that said particular location has been modified by said processor as recited in the claim.

Jeddeloh discloses a logic circuit responsively coupled to said tag memory, said store-in cache memory and said temporary register which routes data from a particular location from said store-in cache memory to said temporary register when said indication is that said particular location has been modified by said processor {*i.e., cache lines marked dirty are selected from cast-out cache and routed to temporary buffer*} [col. 3, lines 35-64].

It would have been obvious to one of ordinary skill in the art, having the teachings of Gallagher and Jeddeloh before him at the time the invention was made, to modify the system of Gallagher to include a temporary register coupled to a store-in cache memory, a first flush buffer store and a second flush buffer store; and a tag memory indicating whether a particular memory location has been modified; and a logic circuit responsively coupled to said tag memory, said store-in cache memory and said temporary register which routes data from a particular location from said store-in cache memory to said temporary register when said indication is that said particular location has been modified by said processor because it would have provided an improved replacement algorithm and better memory access transactions control as taught by

Jeddeloh by providing a short-term storage for dirty (*i.e., modified*) cache lines that are in the process of being written to system memory when L2 cache is full [col. 2, lines 5-14] and by reducing the read latency associated with the search for target data [col.1, lines 59-60, col. 2, line 40] as taught by Jeddeloh.

10. As per claim 13, Gallagher discloses the claimed invention as detailed above per claim 6. However, Gallagher does not specifically teach inhibiting said transferring step if said determining step determines that the data within said particular location was not modified by said processor as recited in the claim.

Jeddeloh discloses inhibiting said transferring step if said determining step determines that the data within said particular location was not modified by said processor {*i.e., clean data not transferred to temporary buffer*} [col. 2, lines 5-10].

As per claim 14, Gallagher discloses the claimed invention as detailed above per claim 6. However, Gallagher does not specifically teach routing the data to the available one of a first flush buffer store and a second buffer store as recited in the claim.

Jeddeloh discloses routing the data to the available one of a first flush buffer store and a second buffer store {*i.e., posted write buffer capable of holding 8 cache lines (i.e., stores)*} [col. 3, lines 35-64].

As per claim 15, Gallagher discloses the claimed invention as detailed above per claim 6. However, Gallagher does not specifically teach rewriting said data to a lower level memory following the transferring step as recited in the claim.

Jeddeloh discloses rewriting said data to a lower level memory following the transferring step {*i.e., all data form temporary buffer a transferred to main memory*} [col. 3, lines 58-61].

It would have been obvious to one of ordinary skill in the art, having the teachings of Gallagher and Jeddeloh before him at the time the invention was made, to modify the system of Gallagher to include discloses inhibiting said transferring step if said determining step determines that the data within said particular location was not modified by said processor; and routing the data to the available one of a first flush buffer store and a second buffer store; and rewriting said data to a lower level memory following the transferring step because it would have reduced the memory latency time experienced by the CPU as taught by Jeddeloh by selecting an existing cache line for replacement based on a status indication [col. 2, lines 1-24] as taught by Jeddeloh.

Claim 20 is rejected as detailed above per claims 12 and 13 above.

Response to Arguments

11. Applicant's arguments filed March 24, 2003 have been fully considered but they are not persuasive. As to the remarks, Applicant asserted that:

(a) Gallagher does not teach or suggest a flush buffer coupled to a store-in cache memory.

Examiner respectfully traverses applicant's arguments for the following reasons. Examiner agrees with Applicant that a store-through cache does not require a flush process as is well know in the art. However, Applicant's assertion that Gallagher does not teach or suggest a flush buffer coupled to a store-in cache memory is clearly erroneous. Examiner would like to point out that the second level cache or cache 26a or L2 cache is a store-in cache as disclosed in column 1, lines 52-57. When a cache line is modified in the L2 cache, the line is flushed to L3 memory as detailed in column 64, lines 40-42, and the line is flushed from L2 cache to L3 memory through the use of an outpage buffer (*i.e., flush buffer*) as detailed in column 67, lines 5-8, and L2 cache write buffers as detailed in column 13, lines 22-25. As such, Gallagher discloses the use of a store-in cache couple to a buffer performing a flush operation or a flush buffer.

(b) the steps of "experiencing, selecting and transferring" of claim 11 are not found in Gallagher.

As per claim 11, Gallagher discloses experiencing a cache miss in response to a searching step as detailed in column 73, lines 11-12; selecting a particular location within said store-in cache to be flushed as detailed in column 73, lines 13-14;

transferring data from said particular location to a flush buffer as detailed in column 73, lines 19-20.

(c) In response to applicant's argument that the examiner's conclusion of obviousness is based upon unsupported conclusion, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this case, the conclusion and motivation is extracted directly from the reference of record. Therefore, the motivation is proper.

(d) The rejection of claims 2 and 12 is proper since Gallagher discloses the use of a store-in cache.

(e) The rejection of claims 4 and 18 is proper since Gallagher discloses L2 cache write buffers handling sequential store operations as detailed an column 13, lines 22-25.

(f) In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the

references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Gallagher discloses a store-in cache coupled to a flush buffer and Jeddeloh discloses a flush buffer coupled to a temporary register for performing a flush operation.

(g) Gallagher does not disclose any cache lines.

As is well known in the art, the sum of the information retrieved and stored in the cache is known as a "cache line". As such, Gallagher discloses "cache lines".

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER

Pierre M. Vital
April 28, 2003